TOSHIBA INTEGRATED CIRCUIT TECHNICAL DATA

TC8570P/F

TC8570P/F

(Universal Asynchronous Receiver Transmitter)

1. INTRODUCTION

The TC8570P/F (UART) is a programmable asynchronous communication LSI. The UART includes a programmable Baud Generator, and is packaged by 40 pin DIP or 44 PIN miniFP. The UART reforms serial-to-parallel conversion about data-character from MODEM, and parallel-to-serial conversion about it from CPU. The CPU can always read status of the UART. The status information include the type and condition of the transfer operations which are transmitted by the UART, and any error information(parity, overrun, framing, or break interrupt). The UART furnishes a complete MODEM control, and processor interrupt function. These functions realize the software architecture to satisfy the user's demands to minimize the CPU occupation time to control communication link.
Also, the UART includes the co-operation mode. When the mode is selected, outputs of data bus and serial transfer are controlled. (Internal operation is not influenced.) It is possible that the composition which use the two UARTs is simple. The two UARTs connect the common CPU bus, and reading from the UART and serial transfer are selected either, writting into the UART is possible at the same time.

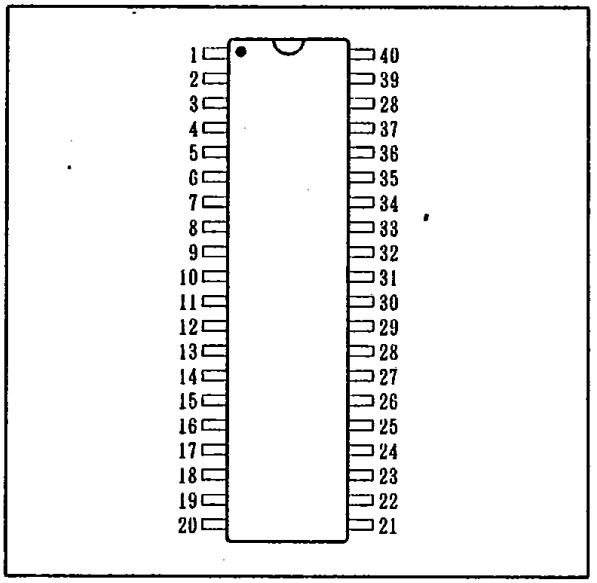
2. FEATURES

- o 8 bit CPU bus compatible
- o Full double buffering
- o Four independent interrupt priority control functions
- o Programmable Baud Generator to divide any input clock by 1 to(2^{16}-1)and to generate the internal 16 X clock
- o Independent receiver clock input
- o MODEM control functions (CTS, RTS, DSR, DTR, CI, and DCD)
- o 5 to 8 bit characters
- o Even, odd, or non-parity bit generation and detection
- o 1, 1.5, or 2 stop bit generation
- o False start bit detection
- o Break character transmission and detection
- o Error detection (break, parity, overrun, and framing error)
- o Complete status reporting capabilities
- o Internal diagnostic capabilities (loopback for communication link, interrupt and receiver error simulation)
- o All inputs are TTL compatible (except /MSEL input)
- o Silicon-Gate CMOS construction
- o Single +5V power supply
- o 40 pin DIP or 44 pin miniFP

3. DESCRIPTION OF PIN

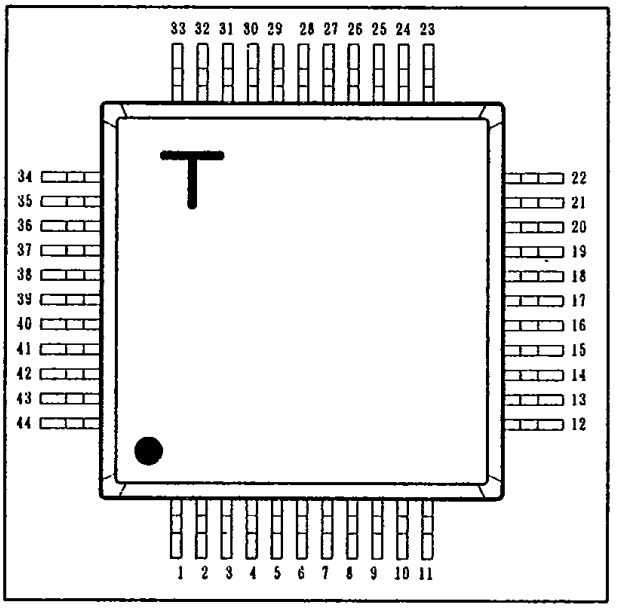
3.1 PIN CONFIGURATION

TC8570P



PIN NO.	IO	PIN NAME	PIN NO.	IO	PIN NAME
1	IO	DB0	21	I	/RD
2	IO	DB1	22	I	RD
3	IO	DB2	23	O	/RDOUT
4	IO	DB3	24	O	CSOUT
5	IO	DB4	25	I	/ALE
6	IO	DB5	26	I	A2
7	IO	DB6	27	I	A1
8	IO	DB7	28	I	A0
9	I	RCLK	29	I	/MASEL
10	I	SIN	30	O	INTRPT
11	O	SOUT	31	O	/OUT2
12	I	CS0	32	O	/RTS
13	I	CS1	33	O	/DTR
14	I	/CS2	34	O	/OUT1
15	O	/BAUDOUT	35	I	RESET
16	I	XIN	36	I	/CTS
17	O	XOUT	37	I	/DSR
18	I	/WR	38	I	/DCD
19	I	WR	39	I	/CI
20	G	GND	40	V	VCC

TC8570F



PIN NO.	IO	PIN NAME	PIN NO.	IO	PIN NAME
1	IO	DB4	23	I	A2
2	IO	DB5	24	I	A1
3	IO	DB6	25	I	A0
4	IO	DB7	26	I	/MASEL
5	I	RCLK	27	O	INTRPT
6	I	SIN	28		NC
7	O	SOUT	29	O	/OUT2
8	I	CS0	30	O	/RTS
9	I	CS1	31	O	/DTR
10	I	/CS2	32	O	/OUT1
11	O	/BAUDOUT	33	I	RESET
12	I	XIN	34	I	/CTS
13	O	XOUT	35	I	/DSR
14	I	/WR	36	I	/DCD
15	I	WR	37	I	/CI
16	G	GND	38	V	VCC
17	V	VCC	39	V	(VCC)
18	I	/RD	40	IO	DB0
19	I	RD	41	IO	DB1
20	O	/RDOUT	42	IO	DB2
21	O	CSOUT	43	IO	DB3
22	I	/ALE	44	IO	DB4

3.2 FUNCTIONAL DESCRIPTION OF TERMINALS

o RESET (Reset) Schmitt Trigger Input
When this input is "H", all registers (except of the Receiver Data, Transmitter Data Buffer, and Baud Generator) and control logic are cleared. Also, output signal of MODEM are cleared. (TABLE-1)

TABLE-1 Reset Functions

Register / Buffer / Signal (Register bit)	Reset Condition 7 6 5 4 3 2 1 0	Reset Control
Interrupt Enable Register	- - - - 0 0 0 0	Reset Input
Interrupt Ident. Register	- - - - - - 0 0	Reset Input
Line Control Register	0 0 0 0 0 0 0 0	Reset Input
MODEM Control Register	0 0 0 0 0 0 0 0	Reset Input
Line Status Register	0 1 1 0 0 0 0 0	Reset Input
MODEM Status Register	X X X X 0 0 0 0	Reset Input
SOUT	High	Reset Input
Receiver Line Status Interrupt	Low	Reset Input/LSR Read
Received Data Ready Interrupt	Low	Reset Input/RDB Read
Transmitter Data Buffer Empty Interrupt	Low	IIR Read / TDB Write
MODEM Status Interrupt	Low	Reset Input/MSR Read
/OUT 1, /OUT 2, /RTS, /DTR	ALL High	Reset Input

-: Always 0 X: External Input

o XIN (Xtal In) Input
This input connects the crystal oscillator or the external clock signal.

o XOUT (Xtal Out) Output
This output is inverted signal of XIN, or connected the crystal oscillator.

o CS0, CS1, /CS2 (Chip Select) Input
When CS0 and CS1 are "H" and /CS2 is "L", the chip is selected and enabled communication between the UART and the CPU. When the co-operation mode (/MSEL=0) is selected, CS1 is not a chip select signal but an input terminal whose contents can be known by reading the Scratchpad Register (it appears D0 bit).

o A0, A1, A2 (Address) Input
These inputs are used to select the register of the UART for the duration of a read or a write operation.

o /ALE (Address Latch Enable) Input
This input is used to latch the address (A0, A1, A2) and chip select (CS0, CS1, /CS2) signals with the edge from "L" to "H". When the address and chip select signals are stable for the duration of a read or a write operation, /ALE ties permanently "L". If these are not stable, it is necessary to be active "L". When the co-operation mode (/MSEL=0) is selected, this terminal is not the latch signal but the output enable signals of DB 7-0 and SOUT.

o WR, /WR (Write) Input
When WR is "H" or /WR is "L" while the chip is selected, it permits the CPU to write data or control words into the selected register of the UART.

o RD, /RD (Read) Input
When RD is "H" or /RD is "L" while the chip is selected, it permits the CPU to read data or status information from the selected register of the UART.

o DB 7-0 (Data Bus) Input/Output
These terminals are 8 bit bidirectional bus to communicate between the UART and the CPU.

o CSOUT (Chip Select Out) Output
This signal indicates that the chip is selected. It can not be done data communication between the UART and the CPU until CSOUT signal is "H".

o /RDOUT (Read Out) Output
Whenever the CPU is reading data from the UART, this signal is "L". This signal can use the enable signal to connect the transceiver to the external data bus.

o /MSEL (Mode Select) Input
When this terminal is "H" or open, the UART is normal operation. If it terminal ties permanently "L" and RESET is "H", it changes the co-operation mode. At this time, /ALE loses a part of latch signals for address (A0, A1, A2) and chip select (CS0, CS1, /CS2). Also, SOUT is "H" during /ALE is "L" and the data bus becomes high-impedance state. The other outputs are not influenced.

o SIN (Serial Input) Input
This terminal is serial data input from the communication link (peripheral device, MODEM, or Data Set).

o RCLK (Receiver Clock) Input
This terminal is input of the 16 X baud rate clock for the receiver section of the UART.

o /BAUDOUT (Baud Output) Output
This terminal supplies the 16 X clock signal of baud rate clock to the transfer section of the UART. The clock rate is equal to the oscillator frequency divided by the value in the Baud Generator Divisor Latches. /BAUDOUT may be used to the standard frequency of receiver section by tying this terminal to RCLK.

o SOUT (Serial Output) Output
This terminal is the composite serial data output for the communication link (peripheral device, MODEM, or Data Set). SOUT is set to the marking (logic 1) state upon a RESET operation. If the co-operation mode (/MSEL=0) is selected, SOUT is set to the marking when /ALE is "L".

o INTRPT (Interrupt) Output
This terminal is set to "H" whenever any one of the following interrupt types has an active "H" condition and is enabled via the Interrupt Enable Register: Receiver Error; Received Data Ready; Transmitter Data Buffer Empty; and MODEM Status. INTRPT signal is reset to "L" upon the appropriate interrupt service or a RESET operation.

o /CI (Call Indicator) Input
When this input is "L", it indicates that the ringing signal has been received by the MODEM or Data Set. /CI signal is a MODEM control function input. The CPU can know its condition by reading CI of the MODEM Status Register. TECI of the MODEM Status Register indicates whether /CI input condition has changed from "L" to "H" since the previous reading of the MODEM Status Register.
Note: If MODEM Status Interrupt is enabled, whenever CI of the MODEM Status Register changes from "H" to "L", an interrupt is generated.

o /DCD (Data Carrier Detect) Input
When this input is "L", it indicates that the data carrier has been detected by the MODEM or Data Set. /DCD signal is MODEM control function input. The CPU can know its condition by reading DCD of the MODEM Status Register. DDCD of the MODEM Status Register indicates whether /DCD input has changed since the previous reading of the MODEM Status Register.
Note: If MODEM Status Interrupt is enabled, whenever DCD of the MODEM Status Register, an interrupt is generated.

o /DSR (Data Set Ready) Input
When this input is "L", it indicates that the MODEM or Data Set is ready to establish the communication link and transfer data with the UART. /DSR signal is a MODEM control function input. The CPU can know its condition by reading DSR of the MODEM Status Register. DDSR of the MODEM Status Register indicates whether /DSR input has changed since the previous reading of the MODEM Status Register.
Note: If MODEM Status Interrupt is enabled, whenever DSR of the MODEM Status Register, an interrupt is generated.

o /CTS (Clear To Send) Input
/CTS signal is a MODEM control function input. The CPU can know its condition by reading CTS of the MODEM Status Register. DCTS of the MODEM Status Register indicates whether /CTS input has changed since the previous reading of the MODEM Status Register.
Note: If MODEM Status Interrupt is enabled, whenever CTS of the MODEM Status Register, an interrupt is generated.

o /OUT 1 (Output 1) Output
This terminal is an output released for user. It can set to an active "L" by programming /OUT 1 of the MODEM Control Register to "H". /OUT 1 signal is set to "H" upon a RESET operation. /OUT 1 signal is forced to its inactive "H" during loop mode operation.

o /OUT 2 (Output 2) Output
This terminal is an output released for user. It can set to an active "L" by programming /OUT 2 of the MODEM Control Register to "H". /OUT 2 signal is set to "H" upon a RESET operation. /OUT 2 signal is forced to its inactive "H" during loop mode operation.

o /RTS (Request To Send) Output
When this terminal is "L", it informs the MODEM or Data Set that the UART is ready to transmit data. /RTS signal is set to "H" upon a RESET operation. /RST signal is forced to its inactive "H" during loop mode operation.

o /DTR (Data Terminal Ready) Output
When this terminal is "L", it informs the MODEM or Data Set that the UART is ready to communicate. /DTR signal is set to "H" upon a RESET operation. /DTR signal is forced to its inactive "H" during loop mode operation.

4. REGISTER

The UART includes ten registers. The user can access and control any of the UART register via the CPU. These registers are used to control the operations of the UART and to transmit and receive data. (TABLE-2)

TABLE-2 Internal Registers

Address	Register / Buffer Name	Data Bit Number 7	6	5	4	3	2	1	0
0 (DLAB=0)	Receiver Data Buffer (RDB)	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
0 (DLAB=0)	Transmitter Data Buffer (TDB)	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0
1 (DLAB=0)	Interrupt Enable Register (IER)	-	-	-	-	EMSI	ELSI	ETDB-EI	ERDRI
2	Interrupt Ident. Register (IIR)	-	-	-	-	-	IID1	IID0	INTF
3	Line Control Register (LCR)	DLAB	SBRK	STCP	EPS	PEN	STB	WLS1	WLS0
4	MODEM Control Register (MCR)	-	-	-	LOOP	OUT2	OUT1	RTS	DTR
5	Line Status Register (LSR)	-	TEMP	TDBE	B D	F E	P E	O E	RDR
6	MODEM Status Register (MSR)	DCD	C I	DSR	CTS	DDCD	TECI	DDSR	DCTS
7	Scratchpad Register (SCR)	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0 CS1
0 (DLAB=1)	Divisor Latch (LS) (DLL)	B 7	B 6	B 5	B 4	B 3	B 2	B 1	B 0
1 (DLAB=1)	Divisor Latch (MS) (DLM)	B15	B14	B13	B12	B11	B10	B 9	B 8

-: Always 0

Note: The RDB and IIR are read-only registers. The TDB is write-only register. Any other registers are possible to read and write, but writting to the Status Registers (LSR, MSR) during the communication are not recommended as these operations are used for diagnostic testing by the interrupt and the simulation of the receiver error.

4.1 LINE CONTROL REGISTER (LCR)

The user can specify the format of the asynchronous data communications exchange via the Line Control Register. In addition to specify the format, the user can refer the contents of the Line Control Register for inspection of the communication link. This construction can be simple the system program, and eliminate the need for separate storage in system memory of the line characteristics.

A2	A1	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	1	DLAB	SBRK	STCP	EPS	PEN	STB	WLS1	WLS0

WLS0, WLS1 (Word Length Select Bit 0, Bit 1)
These 2 bits specify the number of bits in each transmitted or received serial character.

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

STB (Number of Stop Bit)
This bit specifies the number of stop bit in each transmitted or received serial character. If STB is "L", one stop bit is generated in the transmission data. If STB is "H", 1.5 stop bits are generated when a 5-bit word length is selected. If STB is "H", 2 stop bits are generated when either a 6, 7, or 8-bit word length is selected.
The receiver checks the first stop bit only, regardless of the number of stop bits selected.

STB	WLS1	WLS0	Number of Stop Bit
1	0	0	1.5
	0	1	2
	1	0	
	1	1	
0	Non Relations		1

PEN (Parity Enable)
This bit is the Parity Enable bit. When PEN is "H", a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data.

EPS (Even Parity Select)
This bit is the Even Parity Select bit. When PEN is "H" and EPS is "L", an odd number of logic 1's is transmitted or checked in the data word bits and parity bit. When PEN is "H" and EPS is "H", an even number of logic 1's is transmitted or checked.

PEN	ESP	Kind of Parity Bit
1	1	Even Parity
	0	Odd Parity
0	1	Non Parity
	0	

STCP (Stick Parity)
This bit is the Stick Parity bit. When PEN is "H" and STCP is "H", the parity bit (if EPS is "H") is logic 1, or (if EPS is "L") is logic 0.

PEN	STCP	EPS	Parity Bit
1	1	1	1
		0	0

SBRK (Set Break)
This bit is the Break Control bit. When SBRK is "H", the Serial Output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by setting SBRK to "L". The Break Control bit (SBRK) influences only on SOUT and has no effect on the transmitter logic.

DLAB (Divisor Latch Access Bit)
This bit is the Divisor Latch Access Bit. It must be set to a logic 1 to access the Divisor Latches of the Baud Generator during a read or a write operation. It must be set to a logic 0 to access the Receiver Data Buffer, the Transmitter Data Buffer, or the Interrupt Enable Register.

4.2 PROGRAMMABLE BAUD GENERATOR

The UART contents the programmable Baud Generator. The programmable Baud Generator divides input clock by the value that is set by the two 8-bit Divisor Latches (DDL, DDM). The divided frequency is the output signal of /BAUDOUT as 16 X clock of baud rate. The baud rate of transfer data is the frequency of 1/16 output signal.

A2	A1	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	B15	B14	B13	B12	B11	B10	B 9	B 8
0	0	0	B 7	B 6	B 5	B 4	B 3	B 2	B 1	B 0

(DLAB=1)

The frequency of the output signal (baud rate X 16) of /BAUDOUT is follows:

$$\text{Baud Rate X 16 Clock} = B15 \times 2^{15} + B14 \times 2^{14} + B13 \times 2^{13} + B12 \times 2^{12} + \cdots$$
$$\cdots + B3 \times 2^{3} + B2 \times 2^{2} + B1 \times 2 + B0$$

These 16-bit Divisor Latches must be set up during initialization in order to ensure the normally occurrence of the baud rate. Upon writting either upper or lower of the Divisor Latches, the divided value is immediatly loaded into the baud counter. And then, baud counter begins to count.

4.3 Line Status Register (LSR)

This 8-bit register provides the status information to CPU about the data transfer.

A2	A1	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	-	TEMP	TDBE	B D	F E	P E	O E	RDR

-: Always 0

RDR (Received Data Ready)
This bit indicates the Received Data Ready. RDR is set to a logic 1 whenever a complete incoming character has been received and transmitted into the Receiver Data Buffer. RDR is reset to a logic 0 by reading the data in the Receiver Data Buffer.

OE (Overrun Error)
This bit indicates the Overrun Error. If next characters are received into Receiver Data Buffer before the contents of Receiver Data Buffer has been read by the CPU, OE is set to a logic 1. It is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

PE (Parity Error)
This bit indicates the Parity Error. It means that when the Parity Enable bit (PEN) of the Line Control Register is set, the received data did not have the correct even or odd parity as selected by the Even Parity Select bit (EPS) of the Line Status Register. PE is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

FE (Framing Error)
This bit indicates the Framing Error. It means that the received data did not have a valid stop bit. FE is set to a logic 1 whenever the stop bit of the received data is detected as a zero (Spacing level). It is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

BD (Break Detect)
This bit indicates the Break Detect. BD is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for a full transmission time (that is, the total of start bit + data bits + parity bit + stop bit). It is reset to a logic o whenever the CPU reads the contents of the Line Status Register.
Note: OE, PE, FE, and BD are the error conditions that produce the Receiver Status Interrupt whenever any of the corresponding conditions are detected.

TDBE (Transmitter Data Buffer Empty)
This bit indicates the Transmitter Data Buffer Empty. It means that the UART is ready to accept a new character to transfer. When the character is transmitted from the Transmitter Data Buffer to the Transmitter Shift Register, TDBE is set to a logic 1 and the UART occurs the Transmitter Data Buffer Empty Interrupt to the CPU. It is reset to a logic 0 concurrently with the loading of the Transmitter Data Buffer by the CPU.

TEMP (Transmitter Empty)
This bit indicates the Transmitter Empty. TEMP is set to a logic 1 whenever the Transmitter Data Buffer and Transmitter Shift Register are both empty. It is reset to a logic 0 whenever either the Transmitter Data Buffer or Transmitter Shift Register receives a data character.

Bit 7
This bit is always set to logic 0.

4.4 INTERRUPT IDENTIFICATION REGISTER (IIR)

The UART has an interrupt function which allows for complete flexibility in interfacing to all popular microprocessors presently available. The UART prioritizes interrupts into four level to realize minimum expence of software during the data transfer. The prioritizing of interrupt are follows:

Priority 1 : Receiver Line Status
Priority 2 : Received Data Ready
Priority 3 : Transmitter Data Buffer
Priority 4 : MODEM Status

This information indicates a prioritized interrupts pending. The type of interrupt are stored in the Interrupt Identification Register. The Interrupt Identification Register addressed during chip select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. (TABLE-3)

A2	A1	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	-	-	-	-	-	IID1	IID0	INTF

-: Always 0

INTF (Interrupt Flag)
This bit can be used in either a hardwared prioritization or polled environment to indicate whether an interrupt is occurred or not. When this bit set to a logic 0, an interrupt is occurred and the contents of the Interrupt Identification Register may be used as a pointer to the appropriate interrupt service routine. When INTF is set to a logic 1, no interrupt is pending and polling (if used) continues.

IID 0, IID 1 (Interrupt ID Bit 0, Bit 1)
These two bits indicate the kind of the interrupts occurred with the priority. (TABLE-3)

TABLE-3 Interrupt Control Functions

IIR			Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
IID1	IID0	INTF				
0	0	1	-	None	None	-
1	1	0	1	Receiver Line Status	Overrun Error Parity Error Framing Error Break Interrupt	Reading the LSR
1	0	0	2	Received Data Ready	Receiver Data Available	Reading the RDB
0	1	0	3	Transmitter Data Buffer Empty	TDB Empty	Reading the IIR or writting the TDB
0	0	0	4	MODEM Status	Clear to Send Data Set Ready Call Indicator Data Carrir Detect	Reading the MSR

Bit 3-7
These five bits are always set to a logic 0.

4.5 INTERRUPT ENABLE REGISTER (IER)

This register enables the four types of interrupt of the UART separately to activate INTRPT output signal. It is possible to totally disable the interrupt by resetting ERDRI, ETDBEI, ELSI, and EMSI of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions are normal manner, including the setting of the Line Status and MODEM Status Registers.

A2	A1	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	-	-	-	-	EMSI	ELSI	ETDBEI	ERDRI

(DLAB=0)

-: Always 0

ERDRI (Enable Received Data Ready Interrupt)
When this bit sets to a logic 1, the Received Data Ready Interrupt is enabled.

ETDREI (Enable Transmitter Data Buffer Empty Interrupt)
When this bit sets to a logic 1, the Transmitter Data Buffer Empty Interrupt is enabled.

ELSI (Enable Receiver Line Status Interrupt)
When this bit sets to a logic 1, the Receiver Line Status Interrupt is enabled.

EMSI (Enable MODEM Status Interrupt)
When this bit sets to a logic 1, the MODEM Status Interrupt is enabled.

Bit 4-7
These four bits are always set to a logic 0.

4.6 MODEM CONTROL REGISTER (MCR)

This register controls the interface a MODEM or a Data Set or a peripheral device emulating a MODEM.

A2	A1	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	-	-	-	LOOP	OUT2	OUT1	RTS	DSR

-: Always 0

DTR (Data Terminal Ready)
This bit controls the Data Terminal Ready (/DTR) output. When this bit is set to a logic 1, the /DTR output is forced to a logic 0. When this bit is reset to a logic 0, the /DTR output is forced to a logic 1.

RTS (Request To Send)
This bit controls the Request To Send (/RTS) output. When this bit is set to a logic 1, the /RTS output is forced to a logic 0. When this bit is reset to a logic 0, the /RTS output is forced to a logic 1.

OUT 1 (Output 1)
This bit controls the Output 1 (/OUT 1) signal released for user. When this bit is set to a logic 1, the /OUT 1 output is forced to a logic 0. When this bit is reset to a logic 0, the /OUT 1 output is forced to a logic 1.

OUT 2 (Output 2)
This bit controls the Output 2 (/OUT 2) signal released for user. When this bit is set to a logic 1, the /OUT 2 output is forced to a logic 0. When this bit is reset to a logic 0, the /OUT 2 output is forced to a logic 1.

LOOP
This bit supplies a local loop back feature for diagnostic testing of the UART. When LOOP is set to a logic 1, the following occurs: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state, the Serial Input (SIN) is disconnected, the output of the Transmitter Shift Register is "loop back" into the Receiver Shift Register input internally, the four MODEM control inputs (/CTS, /DSR, /DCD, and /CI) are disconnected, the four MODEM control outputs (/DTR, /RTS, /OUT1, and /OUT2) are internally connected to the four MODEM control inputs, and the MODEM control output pins are forced to their inactive states (high). In the diagnostic mode, the transmitted data is immediately received. This feature allows the CPU to verify the transmitting and receiving data paths of the UART. In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational, but the interrupts' source are now the lower four bits of the MODEM Control Register, which are internally connected, instead of the four MODEM control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bit 5-7
These three bits are always set to a logic 0.

4.7 MODEM STATUS REGISTER (MSR)

This register provides the current status of the control lines from the MODEM or peripheral device. In addition to this current status information, the four bits of the MODEM Status Register provide information. These bits are set to a logic 1 whenever a control input from MODEM changes state. They are reset to a logic 0 whenever the CPU reads the MODEM Status Register.

A2	A1	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	0	DCD	C I	DSR	CTS	DDCD	TECI	DDSR	DCTS

DCTS (Delta Clear To Send)
This bit indicates the change of /CTS input. It indicates that /CTS input to the chip has changed state since the last time read by the CPU.

DDSR (Delta Data Set Ready)
This bit indicates the change of /DSR input. It indicates that /DSR input to the chip has changed state since the last time read by the CPU.

TECI (Trailing Edge Call Indicator)
This bit indicates the trailing edge of /CI input. It indicates that /CI input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

DDCD (Delta Data Carrier Detect)
This bit indicates the change of /DCD input. It indicates that /DCD input to the chip has changed state since the last time read by the CPU.
Note: Whenever DCTS, DDSR, TECI, or DDCD is set to a logic 1, MODEM Status Interrupt is generated.

CTS (Clear To Send)
This bit is the complement of the /CTS input. If LOOP of the MODEM Status Register is set to a logic 1, this bit is equivalent to RTS in the MODEM Control Register.

DSR (Data Set Ready)
This bit is the complement of the /DSR input. If LOOP of the MODEM Status Register is set to a logic 1, this bit is equivalent to DTR in the MODEM Control Register1.

CI (Call Indicator)
This bit is the complement of the /CI input. If LOOP of the MODEM Status Register is set to a logic 1, this bit is equivalent to OUT 1 in the MODEM Control Register.

DCD (Data Carrier Detect)
This bit is the complement of the /DCD input. If LOOP of the MODEM Status Register is set to a logic 1, this bit is equivalent to OUT 2 in the MODEM Control Register.

4.8 SCRATCHPAD REGISTER (SCR)

This Read/Write Register does not entirely control the UART. It is intended as a Scratchpad Register to be used by the programmer to hold data temporarily. When the data output control mode (/MSEL=0) is selected, the contents of CS1 appears D0 bit. At this time, CS1 becomes a 1 bit input-port.

A2	A1	A0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	1	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0 / CS1

5. ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS

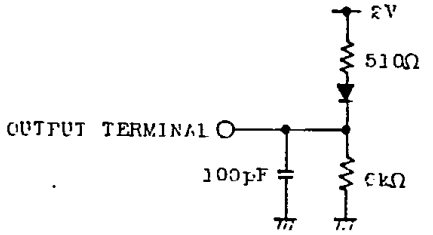
ITEM	SYMBOL	RATING	UNIT
Supply Voltage	VCC	-0.5 to +7.0	V
Input Voltage	VIN	-0.5 to Vcc + 0.5	V
Oparating Temperature	Topr	-40 to +80	°C
Storage Temperature	Tstg	-65 to +125	°C

5.2 DC CHARACTERISTICS

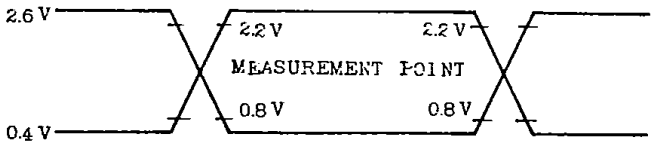
Ta = -40 to +85 °C, Vcc = 5 V ± 10 %

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Low Voltage	VIL		-0.5	0.8	V
Input High Voltage	VIH		2.2	Vcc	V
Output Low Voltage	VOL	IOL = 2.2 mA	-	0.4	V
Output High Voltage	VOH	IOH = -1.1 mA	Vcc-0.4	-	V
Input Leak Current	IIL	VIN = 0 V to Vcc	-10	+10	uA
Supply Current	Icc	fCLK= 4 MHz	-	5	mA

External Load Conditions of Terminal



AC Input Waveform for Test



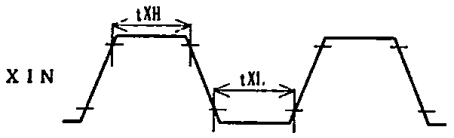
5.3 AC CHARACTERISTICS

Ta = -40 to +85 °C, Vcc = 5 V ± 10 %

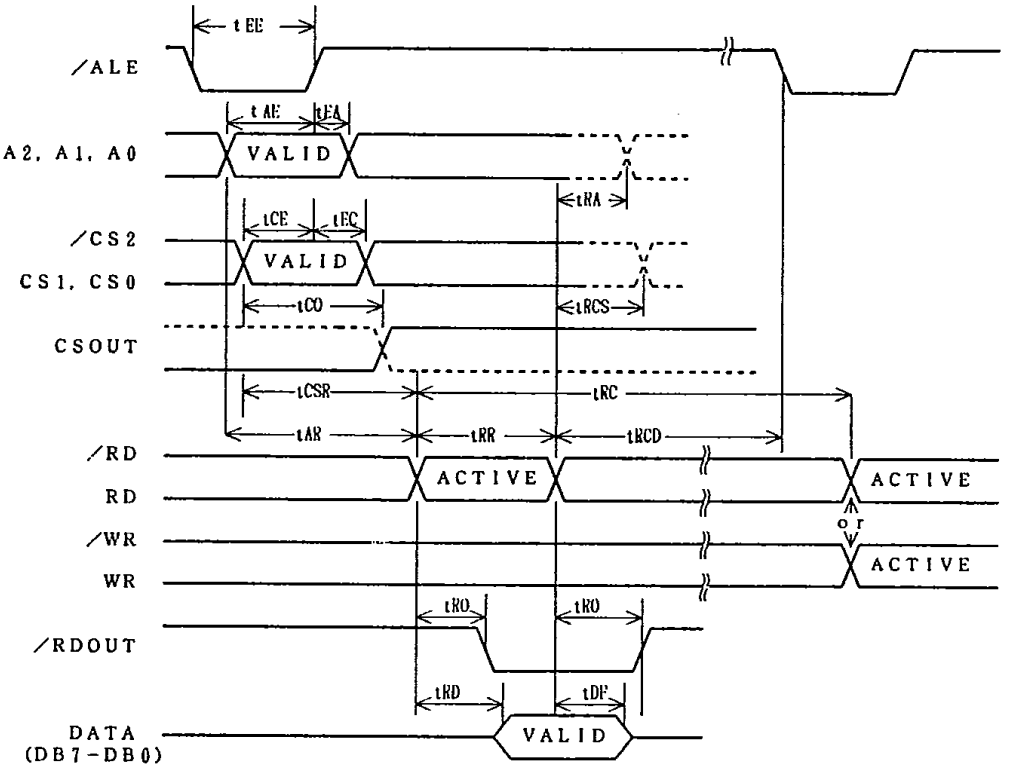
PARAMETER		SYMBOL	MIN	MAX	UNIT
Clock Cycle Time		tXC	250		ns
"High" Clock Pulse Width		tXH	120		ns
"Low" Clock Pulse Width		tXL	120		ns
/ALE Pulse Width		tEE	60		ns
Address Setup Time		tAE	60		ns
Address Hold Time		tEA	10		ns
Chip Select Setup Time		tCE	60		ns
Chip Select Hold Time		tEC	0		ns
RD, /RD Pulse Width		tRR	125		ns
Read Cycle Delay Time		tRCD	175		ns
Read Cycle Time		tRC	360		ns
/RDOUT Delay Time from RD, /RD		tRO		60	ns
Data Delay Time from RD, /RD		tRD		125	ns
Data Float Delay Time		tDF	0	100	ns
WR, /WR Pulse Width		tWW	100		ns
Write Cycle Delay Time		tWCD	200		ns
Write Cycle Time		tWC	360		ns
Data Setup Time from WR, /WR		tDW	40		ns
Data Hold Time from WR, /WR		tWD	40		ns
CSOUT Delay Time	*	tCO		100	ns
Address Setup Time from RD, /RD	*	tAR	60		ns
Address Hold Time from RD, /RD	*	tRA	20		ns
Chip Select Setup Time from RD, /RD	*	tCSR	50		ns
Chip Select Hold Time from RD, /RD	*	tRCS	20		ns
Address Setup Time from WR, /WR	*	tAW	60		ns
Address Hold Time from WR, /WR	*	tWA	60		ns
Chip Select Setup Time from WR, /WR	*	tCSW	50		ns
Chip Select Hold Time from WR, /WR	*	tWCS	20		ns
RESET Pulse Width		tRST	5		us
/BAUDOUT Delay Time		tBAU		125	ns
Receiver					
RDB, LSR Read to INTRPT Reset Delay Time		tRRI		1	us
Stop Bit to INTRPT Delay Time		tRSI	1	1	RCLK
Transmmiter					
TDB Write to INTRPT Reset Delay Time		tTWI		175	ns
Stop Bit to INTRPT(TDBE) Delay Time		tTSI	8	8	/BAUDOUT
IIR Read to INTRPT(TDBE) Reset Delay Time		tTRI		250	ns
MODEM Control					
MCR Write to MODEM Output Delay Time		tMWO		200	ns
MODEM Input Change to INTRPT Delay Time		tMSI		250	ns
MSR Read to INTRPT Reset Delay Time		tMRI		250	ns

*: Applicable only when /ALE is tied low.

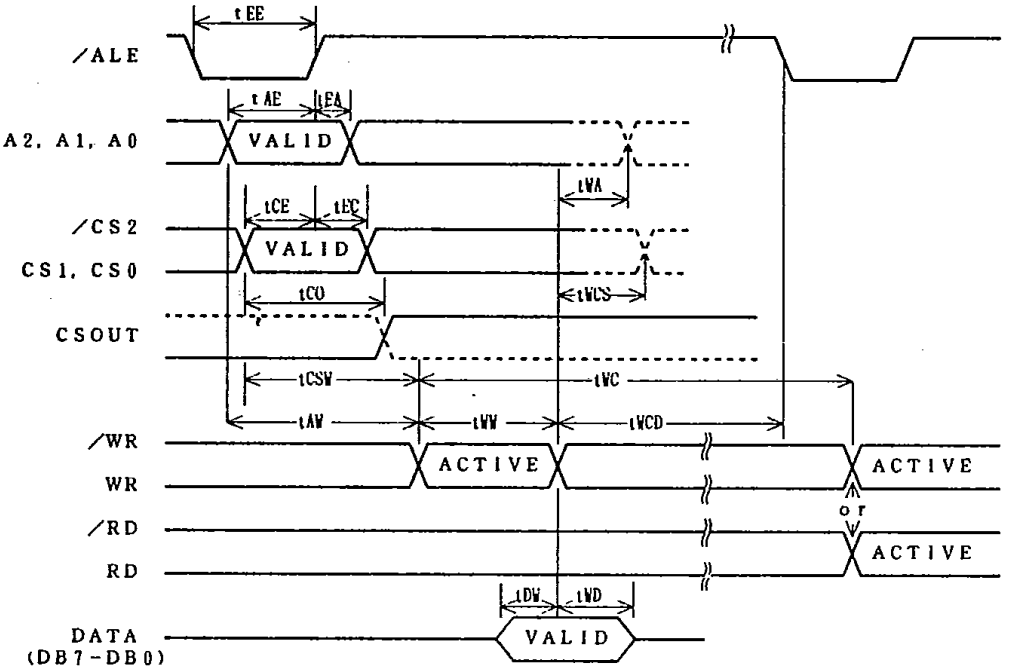
External Clock Input



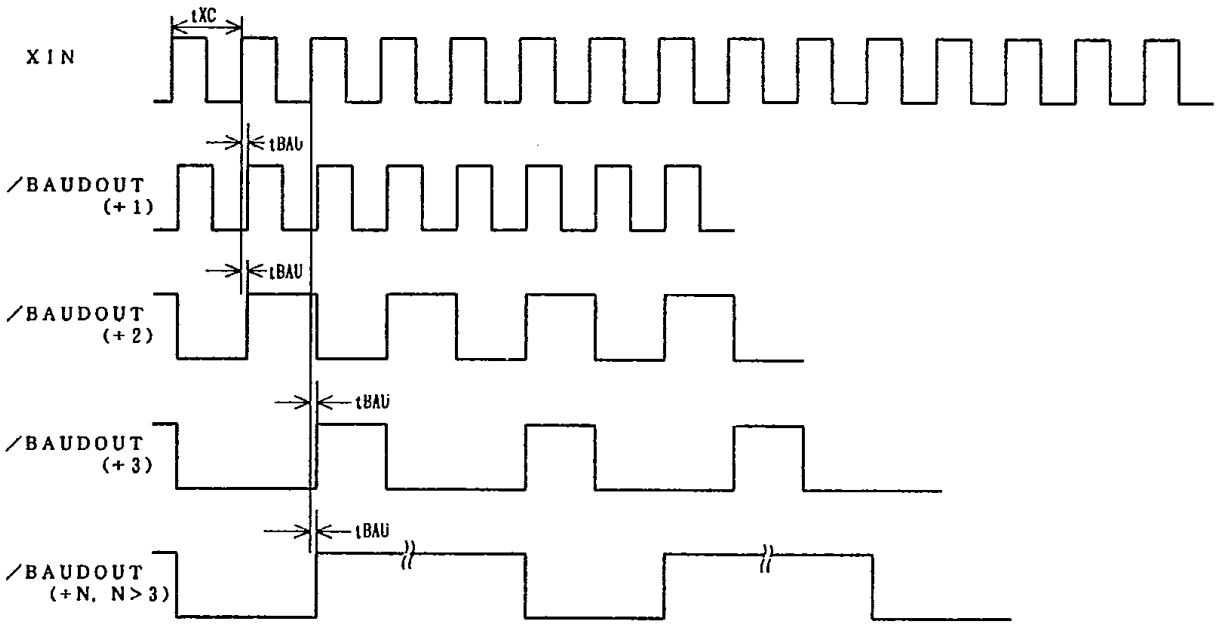
Read Cycle



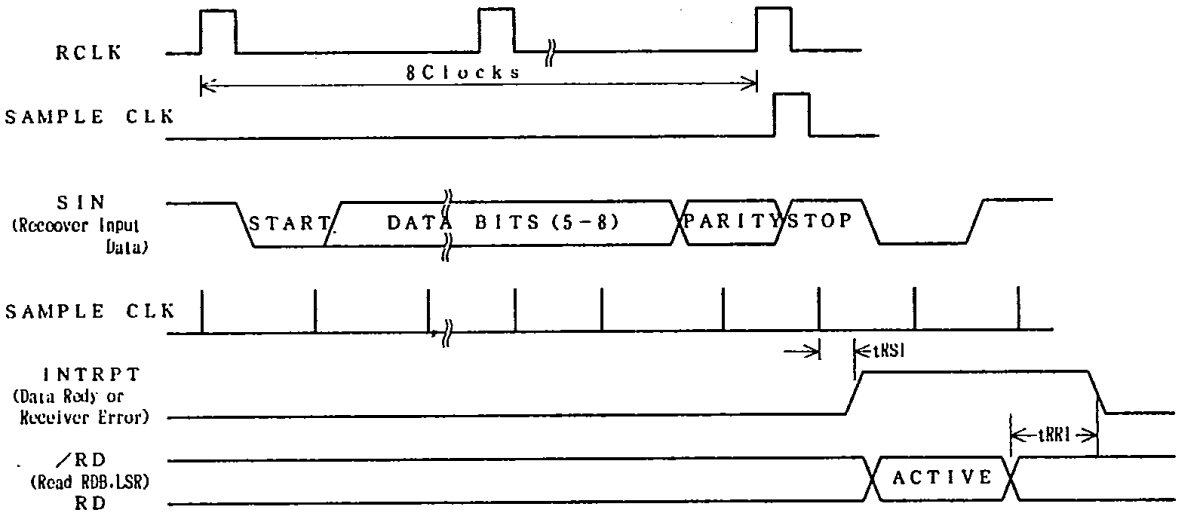
Write Cycle



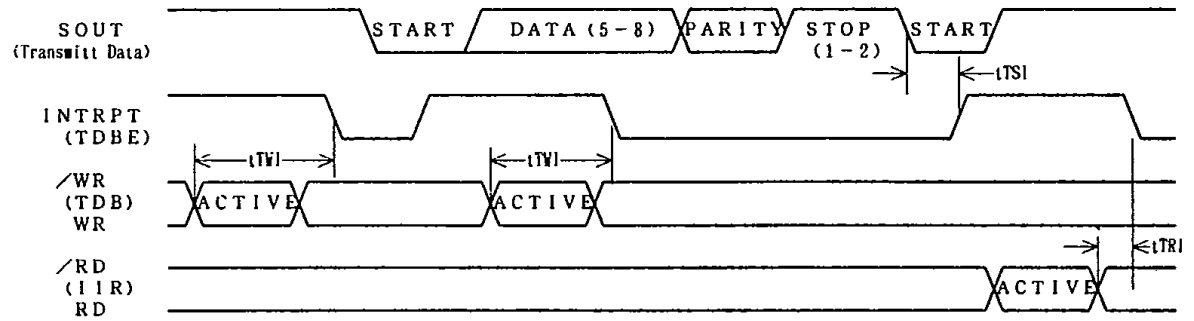
/BAUDOUT Timing



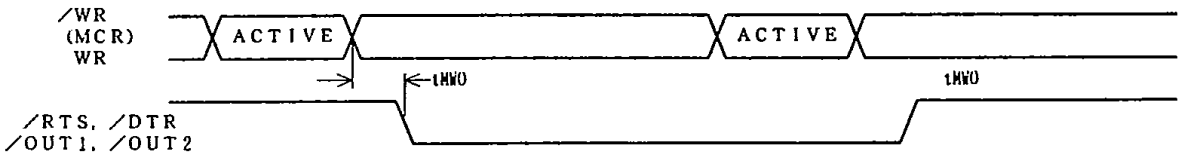
Receiver Timing

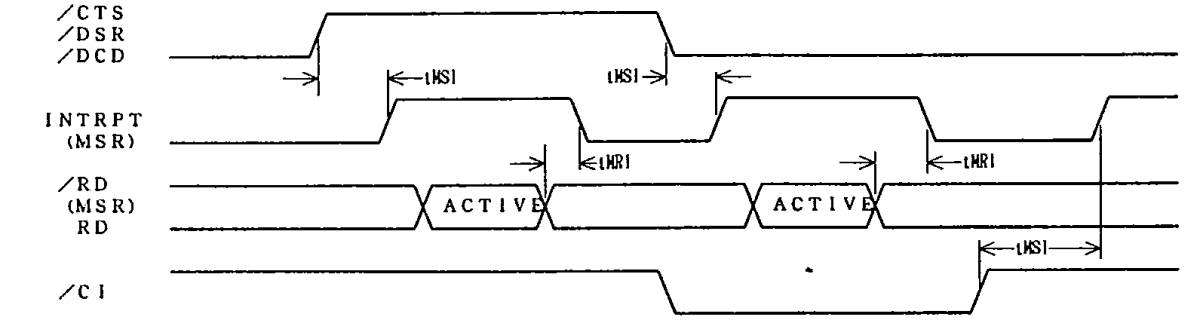


Transmitter Timing



MODEM Control Timing

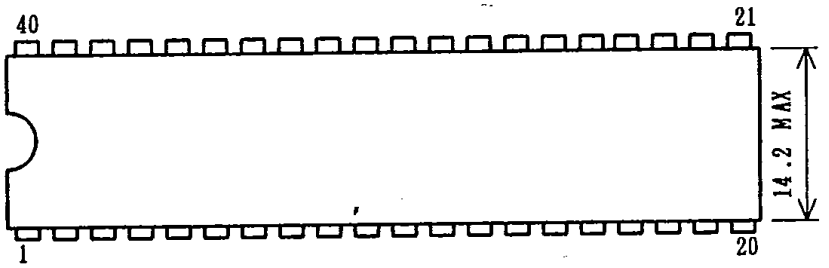


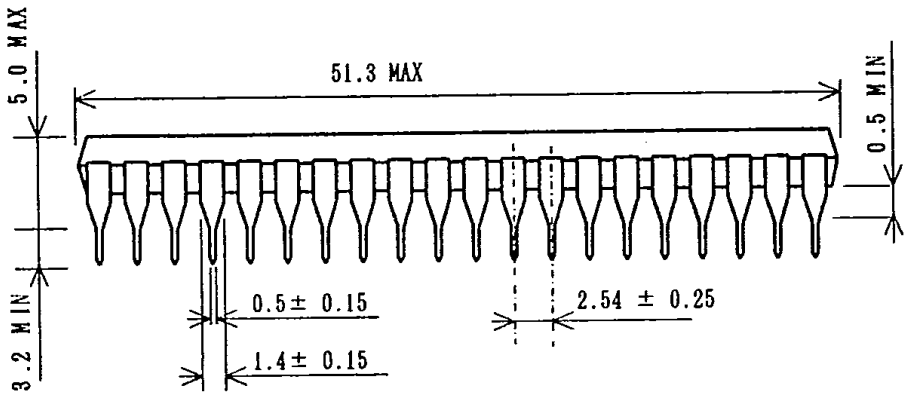


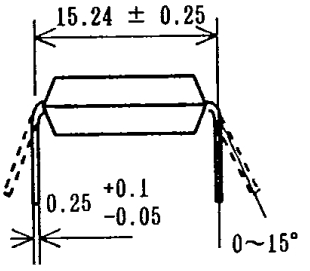
6. PACKAGE OUTLINE

DIP 40 PIN (PLASTIC PACKAGE)

UNIT : mm







mini FP 44 PIN (PLASTIC PACKAGE)

UNIT : mm